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	Filing Date		2004-02-24	
	First Named Inventor	Haw-minn Lu		
	Art Unit	2616		
	Examiner Name	Wellington Chin		
Attorney Docket Number				

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1	PATEL, et al., "Performance of processor-memory interconnections for multiprocessors", IEEE Transactions on Computers, Oct. 1981, pp. 771-780, vol. 30, no. 10, IEEE, US	<input type="checkbox"/>
2	GOKE, et al., "Banyan Network for partitioning multiprocessor systems," First Annual International Symposium on Computer Architecture, December 1973, pp. 21-28, ACM Press, US	<input type="checkbox"/>
3	KUMAR, et al., "Augmented shuffle-exchange multistage interconnection networks". Computer, June 1987, pp.30-40, vol. 20, no. 6, IEEE, US	<input type="checkbox"/>
4	ADAMS, et al., "The Extra Stage Cube: A Fault-Tolerant Interconnection Network for Supersystems," IEEE Transactions on Computers, May 1982, pp. 443-454, vol. 31, no. 5, IEEE, US	<input type="checkbox"/>
5	BENES, "Permutation Groups, Complexes, and Rearrangeable Connecting Networks, Bell System Telephone Journal, July 1964, pp. 1619-1640, vol. 44, AT&T, US	<input type="checkbox"/>
6	HAMID, et al., "A new fast control mechanism for Benes rearrangeable interconnection network useful for supersystems,". Transactions of the Institute of Electronics, Information and Communication Engineers, October 1987, p.997-1008, vol. E70, no. 10, IEICE, Japan.	<input type="checkbox"/>
7	DUDGEON, et al., "Multidimensional Signal Processing,"1984, pp. 60-111, Prentice Hall, Englewood Cliffs, New Jersey."	<input type="checkbox"/>
8	OPPENHIEM, et al., "Digital Signal Processing," 1975, pp. 284-328, Prentice Hall, Englewood Cliffs, New Jersey.	<input type="checkbox"/>

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- ☐ See attached certification statement.
- ☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Haw-minn Lu/	Date (YYYY-MM-DD)	2006-03-28
Name/Print	Haw-minn Lu	Registration Number	55407

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